Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) Reconfigurable signal processing architecture comprising:

a plurality of reconfigurable data processing ~~module~~ modules in which data is input to the plurality of ~~module~~ modules in a packet frame structure including configuration frames and processing frames, each frame including a header section and a data section, the header section having at least one mode selection bit indicating whether the data section of the frame contains reconfiguration data or processing data, and

a single decoder serving the plurality of modules, the single decoder decoding the mode selection bits of the packets and providing respective mode selection signals to the plurality of modules;

wherein each of the ~~module~~ modules is operable in a reconfiguration mode in which the data portion of the packet is used change the data processing performed by the module or a processing mode in which the data portion of the packet is processed by the data processing module, responsive to ~~of~~ the ~~frame header and the mode selection bits~~respective mode selection signal ~~are separated from the data in each frame and are used to control mode selection logic in the module for determining how incoming data is handled~~.

2. Canceled.

3. (Currently Amended) Architecture as claimed in claim ~~2~~1 in which the frame header contains at least one mode selection bit for each of the modules.

4. (Currently Amended) Architecture as claimed in claim 3 in which the single decoder decodes the mode selection bits of the frame header ~~are decoded by a single decoder serving a plurality of modules~~ to provide the respective mode selection signals to the plurality of modules.

5. (Currently Amended) Architecture as claimed in claim 4 in which the ~~decoded~~ mode selection ~~data is~~signals are supplied to the plurality of modules in parallel.

6. (Currently Amended) Architecture as claimed in claim ~~2~~ 1 in which the plurality of modules are connected to each other in series.

7. (Currently Amended) Architecture as claimed in claim 1 in which at least one module of the plurality of modules is additionally operable in a bypass mode in which incoming data is not acted on by the module and in which the header additionally indicates whether or not the one module is to act on the data.

8. (Previously Presented) A radio signal processing apparatus in which signals are processed digitally, in which at least some components of the digital processing section of the apparatus are configurable and incorporate architecture as claimed in claim 1.

9. (Currently Amended) ~~Architecture as claimed in claim 1 in which~~ Reconfigurable signal processing architecture comprising a reconfigurable data processing module in which data is input to the module in a packet frame structure including configuration frames and processing frames, each frame including a header having at least one mode selection bit indicating whether the frame contains reconfiguration data or processing data, and wherein the module is operable in a reconfiguration mode or a processing mode responsive to the frame header and the mode selection bits are separated from the data in each frame and

are used to control mode selection logic in the module for determining how incoming data is handled; and wherein default ~~up~~ configuration data is supplied to the at least one module from a memory outside the at least one module.

10. (Previously Presented) A radio signal processing apparatus according to claim 8 wherein the apparatus is selected from a group consisting of a receiver, a transmitter or a transceiver.

11. (Currently Amended) Architecture as claimed in claim 1 ~~including a plurality of said reconfigurable data processing modules~~ wherein each of the plurality of modules is configured to be operated in a bypass mode in which incoming data is not acted on by the module and in which the frame header additionally indicates whether or not the module is to act on the data.